B. Tech

BCSE 3309/BCSE 3303

Fifth Semester Examination – 2008

COMPUTER ARCHITECTURE AND ORGANIZATION / - I

Full Marks – 70

Time – 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer all questions : 2×10

   (a) Write the basic difference between computer architecture and computer organization.

(b) What do you mean by instruction format ?

(c) What is a BUS ? Explain I/O bus of a computer.

(d) Increasing the number of addressing modes improve the flexibility in writing assembly language programs but reduces the performance. Justify.

(e) What program features justifies the use of cache memory in a hierarchical memory system ?

(f) Explain the advantages and disadvantages of using microprogram and hardwired control unit.

(g) Which register in CPU is responsible for sequencing the control of execution ?

Write its role when a branch instruction is encountered during execution.

(h) Write the steps to retrieve a word from a memory location by the CPU.

(i) Differentiate between page fault and cache miss.

(j) How an interrupt service routine differs from subroutine used in high level language programs ?

2. (a) Explain in brief the Von Neumann architecture with a neat sketch. 5

(b) Give the advantages and disadvantages of single-bus and multi-bus organization. 5

3. (a) Explain the different memory device charactersistics. 5

(b) Explain the following : 5

(i) Locality of reference

(ii) Thrashing

(iii) Address mapping.

4. (a) Explain the difference between bus arbitration using daisy-chaining, polling and independent requesting. Explain with schematic diagram. 5

(b) What do you mean by a cache hit, cache hit time and cache miss penalty ? List and briefly explain the techniques used to improve each of this. 5

5. (a) Justify the use of a hierarchical memory system ? 5

(b) What do you understand by virtual memory ? Distinguish between paging and segmenations. 5

6. (a) A CPU has 16 registers, an ALU with 16 logic and arithmetic functions and a shifter with 8 operations, all connected with a common bus system. 5

(i) Formulate a control word to specify the various microoperations for the CPU.

(ii) Specify the number of bits for each field and give a general encoding scheme for each.

(iii) Show the bits of a control word that specify the microoperatin R7 – R1 + R14.

(b) Design a 7-bit Combinational circuit incrementer for a microprogram sequencer. 5

7. (a) Write the Booth's Algorithm for multiplying two binary numbers in signed-2's complement representation. Give a flow chart scheme. 5

(b) Describe the addition and subtraction process of two decimal numbers in signed-magnitude representation. Suggest a scheme for hardware implementation. 5

8 Write notes on any *two* : 5×2

(a) 8-bit microprocessors

(b) Types of Instructions

(c) IEEE754s.