Total number of printed pages – 7 B. Tech

BCSE 3309/BCSE 3303

Fifth Semester Examination – 2007

COMPUTER ARCHITECTURE AND ORGANIZATION / - I

Full Marks – 70

Time – 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

   (a) Write the basic difference between computer architecture and computer organization.

   (b) List down the difference between shared memory and message passing computers.

P.T.O.

(c) What program features justifies the use of cache memory in a hierarchical memory system ?

(d) Which register in CPU is responsible for sequencing the control of execution ? Write its role when a branch instruction is encountered during execution.

(e) What features designate the 8085 is an 8-bit microprocessor ?

(f) Differentiate between page fault and cache miss.

(g) How an interrupt service routine differs from subroutine used in high level language programs ?

(h) What is the advantage of using cache memory ?

(i) How the divisions can be performed without having any explicit divide instruction in the instruction set of a computer system ?

(j) What are the advantages and disadvantages of high level and assembly language programs ?

2. (a) Define the following : 5

Instruction cycle, Memory cycle, Interrupt cycle and control memory.

(b) Explain the role of following registers in a computer : 5

PC, MAR, MBR, GENERAL PURPOSE REGISTERS, SP, FLAG REGISTER.

3. (a) Explain the detailed organization of a CPU in a digital computer. Define and differentiate between instruction interpretation and instruction sequencing. 5

(b) What is the difference between memory access and memory cycle time ? How they are affected due to destructive and non-destructive readout ? 5

4. (a) Write the different types of microinstruction formats and explain how the degree of parallelism can be improved for generating control signals. 5

(b) What is a pipelined processor ? Develop a set of formulae to compute efficiency and throughput of pipelined processor. What is the speedup gained due to pipelining ? 5

5. (a) Explain with circuit layout for binary division in digital computer. 5

(b) Illustrate Booth's multiplication algorithm with example. 5

6. (a) Discuss the set associative cache memory mapping with an example. 5

(b) A hierarchical cache-main memory sub-system has following specifications : 5

(i) Cache access time of 50 nsec;

(ii) Main storage access time of 500 nsec;

(iii) 80% of memory request are for read;

(iv) hit ratio of 0.9 for read access and the write through scheme is employed. Estimate average access time of the system considering only memory read cycle and for read and write requests.

7. (a) An 8-bit computer has a register R. Determine the values of status bits C,S,Z and V after each of the following instructions. The initial value of register R in each case is hexadecimal 72. The numbers below are also in hexadecimal. 5

(i) Add immediate operand C6 to R

(ii) Add immediate operant 1E to R

(iii) AND immediate operand 8D to R

(iv) Exclusive-OR R with R.

(b) Consider the two 8-bit binary numbers a = 01000001 and B = 10000100 5

(i) Give the decimal equivalent of each number assuming that they are unsigned and they are signed numbers in 2's complement representation.

(ii) Add the two binary numbers and interpret the result assuming that the numbers and the difference are Unsigned and Signed What would the values of status bit C, S, Z and V be ?

8. (a) An arithmetic circuit has two selection variables S_1 and S_0. The arithmetic operations available in the unit are listed below.

Determine the circuit that must be incorporated with a full adder in each stage of the arithmetic unit. 5

S_1	S_0	Cl = 0	Cl = 1
0	0	F = A + B	F = A + B + 1
0	1	F = A	F = A + 1
1	0	F = B	F = B + 1
1	1	F = A + B	F = A + B + 1

(b) Give the infix notation of the following reverse polish expressions : 5

(i) ABCDE */−+

(ii) AB * CD * + EF * +

(iii) AB + C*D+.